

## **COMMON WORDLINE FLASH ARRAY ARCHITECTURE**

### **TECHNICAL FIELD OF THE INVENTION**

**[0001]** The present invention relates generally to memory devices and in particular the present invention relates to a memory device having shared wordlines.

### **BACKGROUND OF THE INVENTION**

**[0002]** Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and flash memory.

**[0003]** A typical flash memory comprises a memory array, which includes a large number of memory cells arranged in blocks. The flash memory is differentiated from other non-volatile memory in that flash memory cells can be erased and reprogrammed in blocks instead of one byte at a time.

**[0004]** The memory blocks each have a row or X-decoder. A column or Y-decoder is shared by multiple memory blocks. An example of a typical memory block architecture is illustrated in Figure 1. This architecture uses an X-decoder for each block of memory.

**[0005]** Figure 1 shows two columns 120 and 121 of memory blocks. Each column 120 and 121 is comprised of eight flash memory array blocks 110 – 115. Each memory array block 110 – 115 has a dedicated X-decoder 101 – 106 respectively. Additionally, each column 120 and 121 has a sense amplifier 130 and 131 that is coupled to a sense amplifier driver 140 and 141.

**[0006]** In order for memory manufacturers to remain competitive, memory designers must constantly increase the density of flash memory devices. This is typically accomplished by reducing the size of the flash memory arrays. The size of the address decoder (e.g., X-decoder, Y-decoder), however, is not shrinking. In fact, as the memory array size is reduced, the proportion of the die that is made up of X-decoders increases. This ultimately limits amount of memory arrays that can fit on one die.

**[0007]** For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a memory array architecture that reduces the amount of die space occupied by address decoders.

## SUMMARY

**[0008]** The above-mentioned problems with address decoder die space and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

**[0009]** The present invention encompasses a memory device having a plurality of memory array blocks. Each memory array block has a plurality of memory cells that are arranged in rows. The rows are coupled together by wordlines. A row decoder is coupled to the plurality of memory array blocks through the wordlines.

**[0010]** Further embodiments of the invention include methods and apparatus of varying scope.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]** Figure 1 shows a block diagram of a typical prior art memory block architecture.

**[0012]** Figure 2 shows a block diagram of one embodiment of the common wordline array architecture of the present invention.

**[0013]** Figure 3 shows a cross-sectional view of a structure suitable for use in fabricating the memory cells of the common wordline array architecture of the present invention.

**[0014]** Figure 4 shows a block diagram of one embodiment of a memory device in accordance with the common wordline array architecture of the present invention.

**[0015]** Figure 5 shows a block diagram of one embodiment of an electronic system of the present invention.

## DETAILED DESCRIPTION

**[0016]** In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

**[0017]** Figure 2 illustrates a block diagram of one embodiment of the common wordline array architecture of the present invention. The memory blocks 203 and 205 are coupled such that they share common wordlines WL0 – WL255 to one X-decoder 201. In one embodiment, the memory blocks are one megabyte memory arrays requiring 256 wordlines. Alternate embodiments use other size memory arrays and, therefore, require different quantities of wordlines.

**[0018]** An externally applied address is input to the X-decoder 201. This circuit 201 activates the desired wordline WL0 – WL255 in response to the input address signals.

**[0019]** Sense amplifiers 207 and 209 are located at the outputs of the memory arrays 203 and 205. The sense amplifier 207 and 209 are used during the read operation to compare currents from the selected memory cells and output the data. The operation of sense amplifiers is well known in the art and is not discussed further.

**[0020]** The embodiment of Figure 2 is a global bit line architecture that uses a Block Pass Select (BPS) driver 230 and 231 to drive the bit line pairs. The global bit line architecture is well known in the art and is not discussed further.

**[0021]** Figure 3 illustrates a cross-sectional view of a structure suitable for use in fabricating the memory arrays of the present invention. The substrate 300 has a first conductivity type (e.g., a p-type conductivity). The substrate 300 includes a lower well region 302 as a semiconductor region having a second conductivity type different from the first conductivity type. For example, the second conductivity type may be opposite the first conductivity type (e.g., an n-type conductivity).

**[0022]** The substrate 300 further includes an upper well region 304 as a semiconductor region having the first conductivity type. The upper well region 304 may be formed in the lower well region 302. The upper well region 304 is isolated from other portions of the substrate 300 having the first conductivity type by the lower well region 302. The lower well region 302 has at least one contact 303 for coupling to a potential node. The upper well region 304 has at least one contact 305 for coupling to another potential node.

**[0023]** For one embodiment, the structure of Figure 3 is a deep n-well 302 formed in a p-type substrate 300. An isolating p-well 304 is located in the n-well 302. Each memory array of Figure 2 is formed into a separate n-well 304 and isolation p-well 304.

**[0024]** In a normal global bit line architecture, a p-well voltage might be 0V for all operations (e.g., read, erase, program) and 0V or V<sub>CC</sub> for an n-well voltage. The common wordline array architecture of the present invention applies different voltages to unselected p-wells and n-wells in order to create an inhibit so as not to disturb the unselected flash cells.

**[0025]** During a program operation, in one embodiment, the unselected p-wells and n-wells have +5V applied in order to inhibit the operation of cells that share the same wordline as a selected cell. During an erase operation, in one embodiment, the unselected p-wells on the same word line have -5V applied and the unselected n-wells on the same word line have 0V applied. During an erase operation, in one embodiment, the unselected p-wells and n-wells have 0V applied. Alternate embodiments may use other inhibit voltages to prevent the unselected flash cells from disturbing the desired operation.

**[0026]** Figure 4 illustrates a block diagram of one embodiment of a memory device in accordance with the common wordline array architecture of the present invention. In this

embodiment, eight memory blocks 403 – 410 share 256 wordlines with one X-decoder 401. In a 64 MB flash memory device, there are eight X-decoders that each share wordlines with eight one megabyte memory blocks. Alternate embodiments that have different memory densities use a different quantity of memory blocks for each X-decoder. The maximum length of one wordline is typically defined by the maximum allowable cells on one wordline without impacting its speed.

[0027] Since the quantity of cell rows in the memory array is increased, the quantity of Y-decoders required to address the array is decreased. This further decreases the amount of die space required for decoders.

[0028] Figure 5 illustrates a functional block diagram of a memory device 500 of one embodiment of the present invention that is coupled to a processor 510. The processor 510 may be a microprocessor, a processor, or some other type of controlling circuitry. The memory device 500 and the processor 510 form part of an electronic system 520. The memory device 500 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

[0029] The memory device includes an array of memory cells 530. In one embodiment, the memory cells are non-volatile floating-gate memory cells and the memory array 530 is arranged in banks of rows and columns.

[0030] An address buffer circuit 540 is provided to latch address signals provided on address input connections A0 – Ax 342. Address signals are received and decoded by a row decoder (X-decoder) 544 and a column decoder (Y-decoder) 546 to access the memory array 530. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 530. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

[0031] The memory device 500 reads data in the memory array 530 by sensing voltage or current changes in the memory array columns using sense/latch circuitry 550. The sense/latch circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 530. Data input and output buffer circuitry 560 is included for

bi-directional data communication over a plurality of data connections 562 with the controller 510. Write circuitry 555 is provided to write data to the memory array.

[0032] Control circuitry 570 decodes signals provided on control connections 572 from the processor 510. These signals are used to control the operations on the memory array 530, including data read, data write, and erase operations. In one embodiment, the control circuitry 570 executes the error correction schemes of the present invention. The control circuitry 570 may be a state machine, a sequencer, or some other type of controller.

[0033] The flash memory device illustrated in Figure 5 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

[0034] The above-described embodiments of the present invention are discussed with reference to a flash memory device, including both NAND and NOR-type flash devices. However, the present invention is not limited to any one type of memory device. Any memory device that would benefit from sharing wordlines to reduce decoder area is encompassed by the present invention.

## CONCLUSION

[0035] In summary, a common wordline architecture uses one X-decoder with multiple memory blocks sharing the same wordlines. This decreases the quantity of X and Y-decoders required and improves memory device performance due to a die size reduction.

[0036] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.